Nonlinear Modeling and Verification of MMIC Amplifiers Using the Waveform-Balance Method

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Abstract—**An accurate nonlinear MESFET model, a new amplifier large-signal simulation algorithm, and a reliable model verification approach are presented. The MESFET model is derived from S-parameter characterization of the MESFET using a wide range of bias voltages. This model is shown to be accurate at various frequencies, bias voltages, and input power levels. The nonlinear simulation utilizes a circuit analysis algorithm which we call the waveform-balance method. The algorithm is a hybrid method which uses both time-and frequency-domain analysis. Unlike the popular harmonic balance method, the solution is optimized in the time domain, where the closed-form error gradient matrix (Jacobian matrix) is calculated. This new algorithm is shown to have good convergence speed. To verify the MESFET model, two MMIC single-stage power amplifiers and test patterns of their matching circuits are designed. The load and source impedances presented to the MESFETs in the amplifier circuits are accurately determined by on-wafer S-parameter measurements of the amplifiers' matching circuits. These S-parameter data are directly used in the simulation of the MMIC amplifiers. The simulation results agree well with the measurement data.**

I. INTRODUCTION

IN THE PAST few years, many nonlinear MESFET models have been reported. Commercial nonlinear analysis software has also become available. However, despite the need for CAD tools for MMIC power amplifier disigns, nonlinear MESFET models have not been widely used in industry. There are three major reasons that have prevented nonlinear MESFET models from becoming practical CAD tools: 1) the accuracy of these models is questionable; 2) the lack of verification; and 3) the relatively long computation time required. In this work, we present a nonlinear MESFET model which is shown to be accurate at various frequencies, bias voltages, and input power levels. The nonlinear simulation utilizes an efficient algorithm called the waveform-balance method. This method is based on an algorithm originally proposed for diode mixer analysis [1]. To establish the validity of this approach, a reliable on-wafer characterization scheme is used for model verification.

Many nonlinear MESFET models [2]–[4] are based on curve-fitting a device's channel current to the measured dc $I-V$ curves. These dc fitted models ignore the fact that the MESFET's transconductance, G_m, and output resistance, R_o, are frequency dispersive in the low-frequency range [5], [6]. This results in higher predicted gain and output power because the dc G_m and R_o values of the MESFET are higher than RF values. In this work, the MESFET model is developed from S-parameter measurements at various bias voltages. Since this model is based on the high-frequency RF data, the low-frequency dispersion characteristics of G_m and R_o do not affect the accuracy of the model.

The waveform-balance method is used here for the first time to analyze MMIC power amplifiers. The method is different from the well-known harmonic balance method. Here, the steady-state solution is sampled and optimized in the time domain rather than in the frequency domain. In this new method, the closed-form error gradient matrix (Jacobian matrix) required in the optimization procedure in calculated in the time domain, whereas in the harmonic balance method the error gradient matrix can only be calculated numerically in the frequency domain. The new method is shown in this work to have good accuracy and convergence rate.

In the past, MESFET nonlinear models are often verified by measuring the power performance of a MESFET device mounted in a test fixture. In the conventional approach, reliable measurement data are difficult to obtain due to the uncertainties in determining the tuner and fixture losses, and the impedances presented to the MESFET. In our verification approach, the nonlinear model is verified by comparing the simulation results of the single-stage MMIC amplifiers with the measured data. The S parameters of the amplifiers' input and output matching circuits are first accurately measured using the on-wafer RF probes. These data are then entered into the simulation program for the complete amplifier simulation. With this approach, the uncertainties of the matching circuit's

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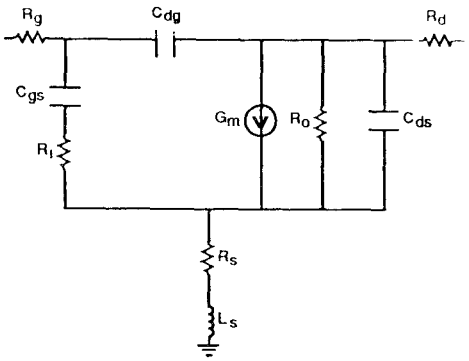


Fig. 1. Small-signal equivalent circuit of the MESFET.

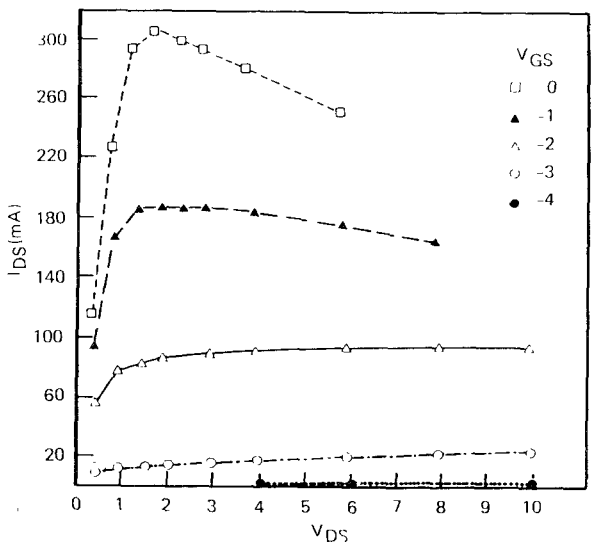


Fig. 2. dc $I-V$ curves of the 1.2 mm MESFET.

impedances and loss are minimized, and the MESFET model is verified with a high degree of confidence.

II. Nonlinear MESFET Modeling

The nonlinear RF fitted model is developed in the following steps.

1) Measure the MESFET's S parameters over a wide range of bias voltages using on-wafer probes.
2) Fit the MESFET small-signal equivalent (Fig. 1) circuit to the S parameters measured in step 1. The values of R_g, R_d, R_s, L_g, L_d, and L_s (in Fig. 1) are fixed when the equivalent circuit is fitted.
3) The MESFET's voltage-dependent elements versus bias voltage curves are plotted out. Fig. 2 shows the dc $I-V$ curves of the device. Figs. 3–8 are the G_m, R_o, C_{gs}, C_{ds}, C_{dg}, and R_i curves for a 1200 μm $\times$ 0.5 μm ion-implanted MESFET.
4) Empirical expressions of the nonlinear elements, $I_{ch}(V_g, V_d)$, and $C_{gs}(V_g, V_d)$ of the large-signal equivalent circuit (Fig. 9) are fitted to the curves of Figs. 3–5. The expression for C_{gs} is

$$C_{gs}(V_g, V_d) = \left[C_0/(1 - V_g/V_b)^r\right](1 + b \cdot V_d) + d \quad (1)$$

where C_0, V_b, r, b, and d are the fitting parameters.

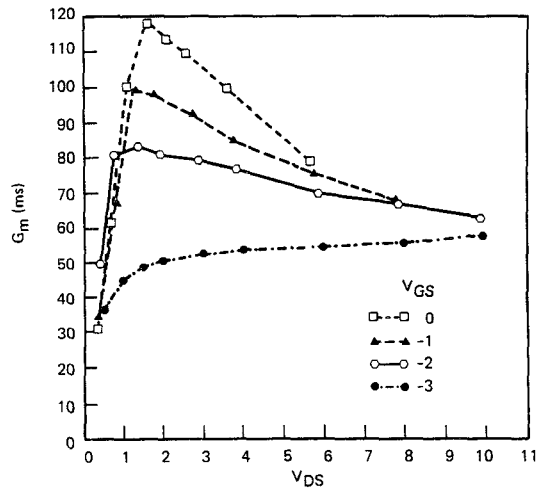


Fig. 3. G_m versus V_{GS} and V_{DS} curves.

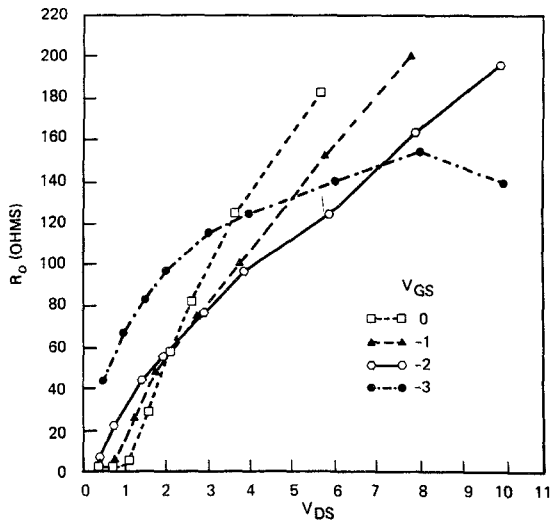


Fig. 4. R_o versus V_{GS} and V_{DS} curves.

The expression for I_{ch} is

$$I_{ch}(V_g, V_d) = X_5(V_g + X_2)^{X_8} \tanh(X_1 V_d) - (X_3 + X_4 V_g)^2 V_d + V_d/(X_6 + X_7 V_d) \quad (2)$$

where X_1 through X_8 are the fitting parameters. These fitting parameters are optimized such that the partial derivatives of I_{ch}, $\partial I_{ch}/\partial V_g$ and $\partial I_{ch}/\partial V_d$, are matched to the G_m and R_o curves.

The $I-V$ curves predicted by the "RF model" developed thus far do not match the measured dc $I-V$ curves. Therefore, the dc drain current under a large-signal RF driving condition can only be approximated by the following approach. First, a separate dc model for the device's channel current is needed to calculate the dc quieseent drain current, I_{DQ}, before RF driving. This model is developed by fitting an expression such as the one in [3] or [4] to the measured dc $I-V$ data. The dc drain currents

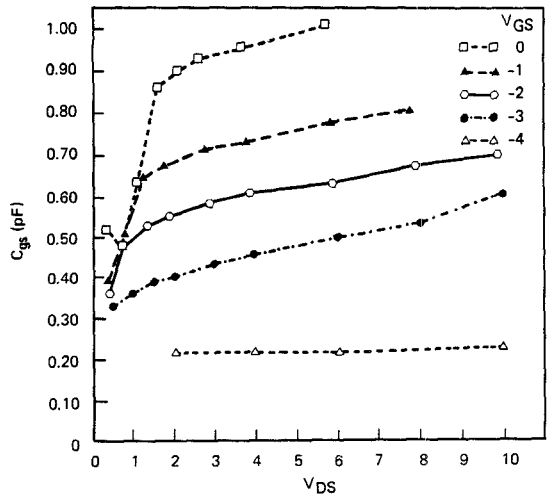


Fig. 5. C_{gs} versus V_{GS} and V_{DS} curves.

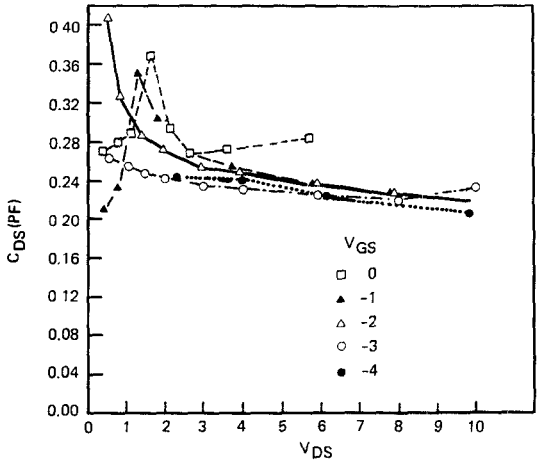


Fig. 6. C_{ds} versus V_{GS} and V_{DS} curves.

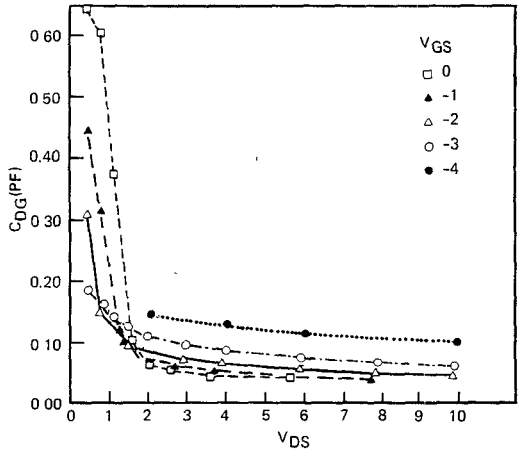


Fig. 7. C_{dg} versus V_{GS} and V_{DS} curves.

under the RF driving condition is then approximated as

$$I_{DC} = I_{DQ} + \Delta I \tag{3}$$

where

$$\Delta I = I_{\mathrm{RF2}} - I_{\mathrm{RF1}}. \tag{4}$$

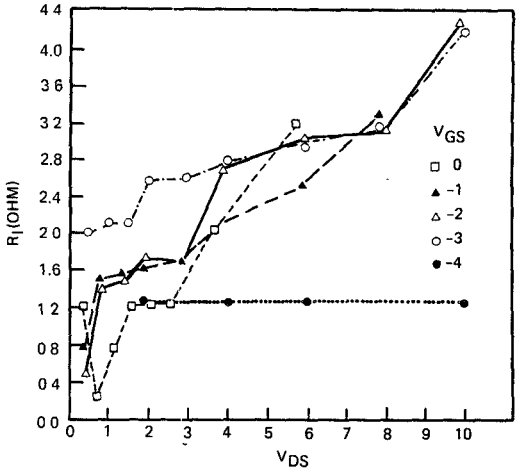


Fig. 8. R_i versus V_{GS} and V_{DS} curves.

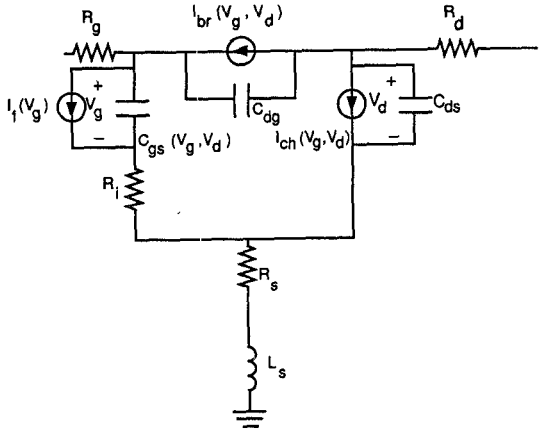


Fig. 9. MESFET large-signal equivalent circuit.

I_{RF1} and I_{RF2} are the dc drain currents predicted by the "RF model" (using (2)) before and after RF driving, respectively.

In general, the G_m curves can be fitted closely. However, the R_o curves are difficult to fit over the entire voltage range. To ensure the accuracy of the model under the normal amplifier bias conditions (i.e., $V_G = -1$ to -3 V, $V_D = 5$ to 8 V), this region of the R_o curves is fitted closer by using a larger weighting factor during the fitting procedure.

The other elements, C_{dg}, C_{ds}, and R_i, also appear to be nonlinear. However, to smplify the analysis, their values are assumed to be only bias voltage dependent. Their values depend on the dc bias voltages but do not change with instantaneous ac voltages, $V_g(t)$ and $V_d(t)$.

5) The breakdown current, I_{br}, and the gate forward current, I_f, are fitted to the pulse measured gate current versus gate and drain voltage data. The expression for I_{br} is

$$I_{br}(V_g, V_d) = I_2 \cdot \exp(r_1 \cdot V_d - r_2 \cdot V_g) \tag{5}$$

where I_2, r_1, and r_2 are the fitting parameters.

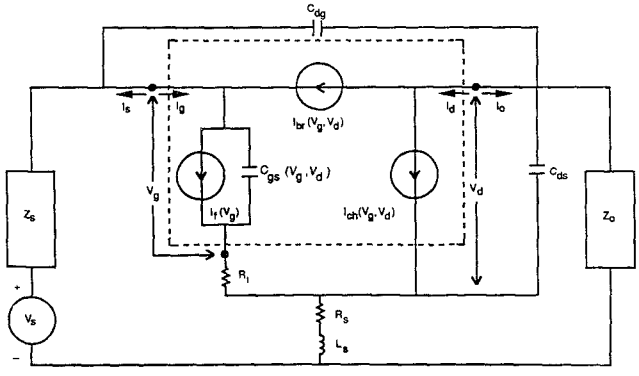


Fig. 10. Nonlinear MESFET amplifier circuit.

III. Waveform-Balance Method

The waveform-balance algorithm is a hybrid method which uses both time- and frequency-domain analysis. In this method, the amplifier circuit is first decomposed into linear and nonlinear subcircuits. The steady-state voltages at the nodes connecting the linear and the nonlinear subcircuits are first sampled in the time domain. The resulting voltage amplitudes at each sampling point are then optimized using an iterative scheme to satisfy the current balance condition. In this procedure, the error gradient matrix in the time domain is calculated in closed form.

A. Problem Formulation

To understand the waveform-balance algorithm, consider the nonlinear amplifier circuit shown in Fig. 10. The nonlinear subcircuit is enclosed by dotted lines in Fig. 10. The nonlinear elements are $I_f(V_g)$, $C_{gs}(V_g, V_d)$, $I_{ch}(V_g, V_d)$, and $I_{br}(V_g, V_d)$, which are represented by explicit nonlinear expressions. We are seeking the steady-state voltages V_g and V_d at the nodes connecting the linear and nonlinear subcircuits that minimize the $2N$-point error function:

$$F_i = I_{s_i} + I_{g_i}$$
$$F_{N+i} = I_{o_i} + I_{d_i} \qquad \text{for } i = 1, 2 \cdots N \tag{6}$$

where N is the number of sampling points per period of the fundamental frequency. I_{s_i} is the amplitude of the current $I_s(t)$ (shown in Fig. 10) evaluated at each sampling point. I_{g_i}, I_{o_i}, and I_{d_i} are interpreted in the same manner.

Fig. 11 is the flowchart of the waveform-balance algorithm. The algorithm starts with an initial guess of V_{g_i} and V_{d_i} (V_{g_i} and V_{d_i} are the amplitudes of $V_g(t)$ and $V_d(t)$ at each sampling point) using small-signal analysis. Currents (at each sampling point) flowing into the nonlinear subcircuit are then calculated as

$$I_{g_i} = I_f(V_{g_i}) + C_{gs}(V_{g_i}, V_{d_i}) \times V'_{g_i} - I_{br}(V_{g_i}, V_{d_i})$$
$$I_{d_i} = I_{ch}(V_{g_i}, V_{d_i}) + I_{br}(V_{g_i}, V_{d_i}) \qquad \text{for } i = 1, 2, \ldots, N \tag{7}$$

where V'_{g_i} is the time derivative of V_g at each sampling point. To calculate the currents flowing into the linear

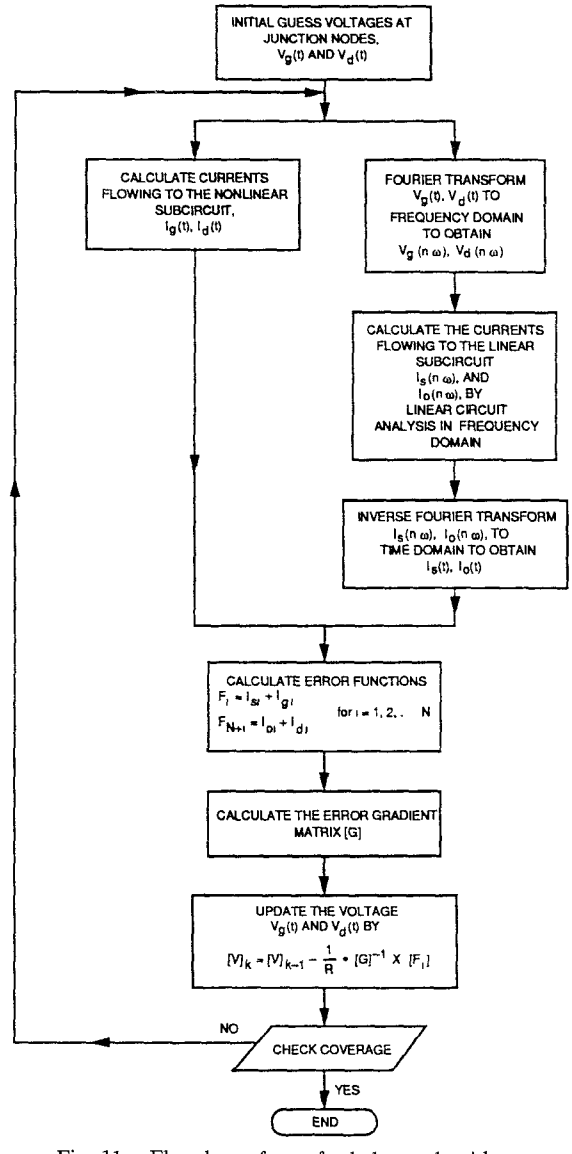


Fig. 11. Flowchart of wavefor-balance algorithm.

subcircuit (I_{s_i} and I_{o_i}), the voltages V_g and V_d are first Fourier-transformed using a discrete transform (FFT) to the frequency domain, and are then applied to the linear subcircuit. The resulting currents are then calculated by linear circuit analysis. They are subsequently converted back to the time domain by the inverse Fourier transform (IFT).

Next, the error function is calculated using (6). In each interation, the time-domain sampled voltages, V_{g_i} and V_{d_i}, are updated via

$$[V]_k = [V]_{k-1} - 1/R \cdot [G]^{-1} \times [F_i] = [V]_{k-1} - 1/R \cdot [\Delta V] \tag{8}$$

where $[V] = [V_{g_1}, V_{g_2}, \cdots, V_{g_N}, V_{d_1}, V_{d_2}, \cdots, V_{d_N}]^t$, $[F_i] = [F_1, F_2, \cdots, F_{2N}]^t$, the superscript k is the kth iteration, and R is the relaxation factor. $[G]$ is the $2N \times 2N$ error gradient matrix, which will be obtained by the method described next. The value of the relaxation factor R affects

the convergence speed. The criteria for choosing the value of R are discussed in [1].

B. Error Gradient Matrix Calculation

The error gradient matrix $[G]$ can be written as $[G]=[G_e]+[G_n]$, where $[G_e]$ and $[G_n]$ are the error gradient matrices contributed by the linear and nonlinear subcircuits, respectively. These matrices can be decomposed into submatrices as shown below:

$$[G_n]=\begin{bmatrix}[\partial I_g/\partial V_g] & [\partial I_g/\partial V_d]\\ [\partial I_d/\partial V_g] & [\partial I_d/\partial V_d]\end{bmatrix}$$
$$[G_e]=\begin{bmatrix}[\partial I_s/\partial V_g] & [\partial I_s/\partial V_d]\\ [\partial I_o/\partial V_g] & [\partial I_o/\partial V_d]\end{bmatrix} \tag{9}$$

To see how $[G_n]$ and $[G_e]$ are calculated, consider first $[G_n]$, which is the error gradient matrix due to the nonlinear subciruit. This matrix can be evaluated in closed form. For example, the (i, j) element of the submatrix $[\partial I_d/\partial V_d]$ is calculated as

$$\partial I_{d_i}/\partial V_{d_j}=\partial I_{ch}(V_{g_i},V_{d_i})/\partial V_{d_j}+\partial I_{br}(V_{g_i},V_{d_i})/\partial V_{d_j}. \tag{10}$$

The other three submatrices of $[G_n]$ are calculated using the same principle.

To calculate $[G_e]$ (error gradient matrix due to the linear subcircuit), consider the submarix $[\partial I_s/\partial V_g]$ of $[G_e]$ as an example:

$$[\partial I_s/\partial V_g]=\begin{bmatrix}\partial I_{s_1}/\partial V_{g_1} & \partial I_{s_1}/\partial V_{g_2} & \cdots & \partial I_{s_1}/\partial V_{g_N}\\ \partial I_{s_2}/\partial V_{g_1} & \partial I_{s_2}/\partial V_{g_2} & \cdots & \cdot\\ \cdot & \cdot & \cdots & \cdot\\ \cdot & \cdot & \cdots & \cdot\\ \cdot & \cdot & \cdots & \cdot\\ \partial I_{s_N}/\partial V_{g_1} & \cdot & \cdots & \partial I_{s_N}/\partial V_{g_N}\end{bmatrix}. \tag{11}$$

The first column of $[\partial I_s/\partial V_g]$ contains the ratios of the perturbation of I_s at each sampling point with respect to the perturbation of V_g at the first sampling point. To calculate these ratios, the time-domain series $\{\partial V_{g_1},0,0,\cdots,0\}$ of N points is converted to the frequency domain by FFT. This perturbation is then applied to the linear subcircuit, as shown in Fig. 12, and the resulting current is transformed back to the time domain as $\{\partial I_{s_1}, \partial I_{s_2},\cdots,\partial I_{s_N}\}$. This series is equal to $\{\partial I_{s_1}/\partial V_{g_1}, \partial I_{s_2}/\partial V_{g_1},\cdots,\partial I_{s_N}/\partial V_{g_1}\}$ by making $\partial V_{g_1}=1$. The second column of $[\partial I_s/\partial V_g]$ contains the ratios of the perturbation of I_s with respect to the perturbation of V_g at the second sampling point. It can be shown that the second column is related to the first column via (12) due to the time invariance property of the linear circuit:

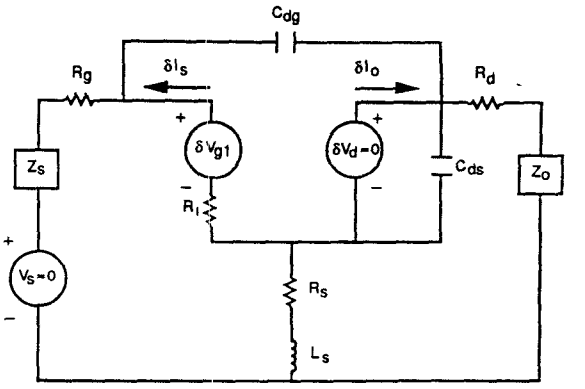


Fig. 12. Circuit diagram for calculating $[\partial I_s/\partial V_g]$.

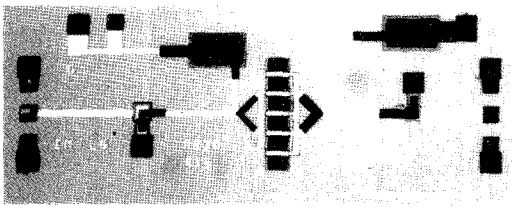
$$\partial I_{s_{i+1}}/\partial V_{g_2}=\partial I_{s_i}/\partial V_{g_1} \quad \text{for } i=1,2,3,\cdots,N-1$$
$$\partial I_{s_1}/\partial V_{g_2}=\partial I_{s_N}/\partial V_{g_1} \quad \text{when } i=N. \tag{12}$$

The remaining columns of $[\partial I_s/\partial V_g]$ are obtained by shifting the first column accordingly. The three other submatrices of $[G_e]$ can be constructed by the same method. The matrix $[G_e]$ does not change from iteration to iteration. Therefore, it needs to be calculated only once.

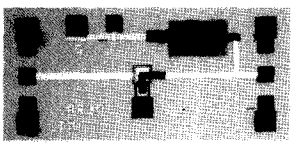
For amplifier analysis, normally 16 sampling points, $(N=16)$ is sufficient. With 16 sampling points eight harmonic voltages and the respective output powers can be calculated.

IV. Model Verification

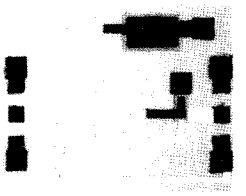
To verify the nonlinear modeling approach, two different single-stage MMIC amplifiers (A and B) were designed and tested. These two amplifiers are fabricated in two different wafer runs. In each case, the amplifier's matching circuit drop-outs and its MESFET device drop-out are fabricated on the same wafer along with the amplifier (Figs. 13 and 14). Amplifier A uses the 1200 μm$\times$0.5 μm ion-implanted MESFET with characteristics given in Figs. 2–8. Amplifier B uses a 980 μm$\times$0.5 μm ion implanted MESFET whose configuration is different from the one used in amplifier B. The nonlinear models for these two devices are developed by characterizing the MESFET drop-outs using on-wafer probes. Since the test FET and the amplifier are fabricated on the same wafer and are located very close to each other, the uncertainty in comparing the simulated data and measured data due to the process variation is reduced. To simulate the amplifiers, the S parameters of the input and output matching circuits need to be known. These S parameters are accurately measured by on-wafer probing of the matching circuit drop-outs. In the present analysis, the input and output terminations for the higher harmonics are assumed to be 50 Ω. These amplifiers are first characterized on-wafer for their small signal gain. They are then diced and mounted on a test fixture for power testing. Since the power testing is done on a 50 Ω scaler system, the measured power data are very accurate. The uncertainty is believed to be less than 0.5 dB.



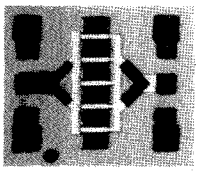
MMIC SINGLE STAGE AMPLIFIER



INPUT MATCHING CIRCUIT

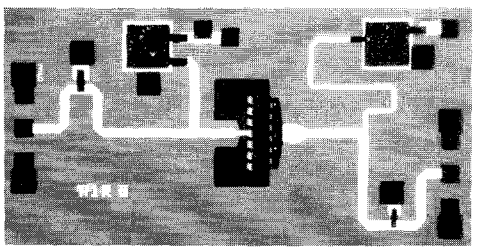


OUTPUT MATCHING CIRCUIT

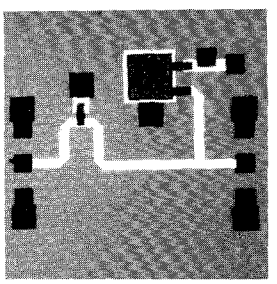


MESFET DROP-OUT

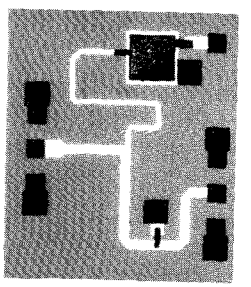
Fig. 13. Photographs of amplifier A and its drop-outs.



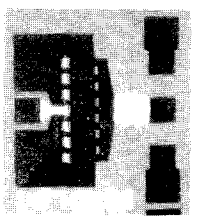
MMIC SINGLE STAGE AMPLIFIER



INPUT MATCHING CIRCUIT



OUTPUT MATCHING CIRCUIT



MESFET DROP-OUT

Fig. 14. Photographs of amplifier B and its drop-outs.

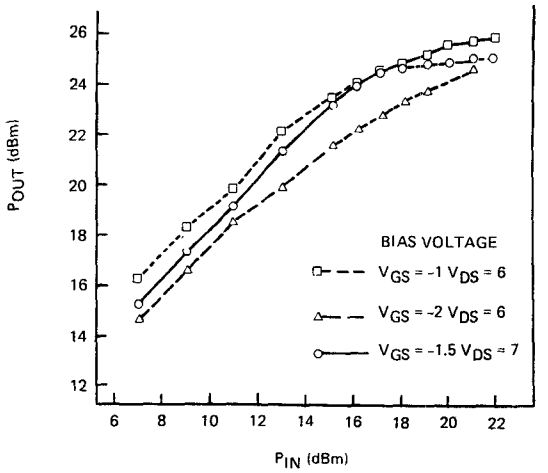


Fig. 15. Simulated P_{out} versus P_{in} curves of amplifier A at 10.65 GHz.

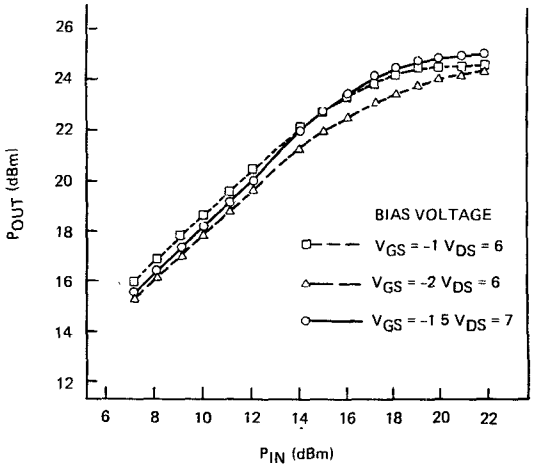


Fig. 16. Measured P_{out} versus P_{in} curves of amplifier A at 10.65 GHz.

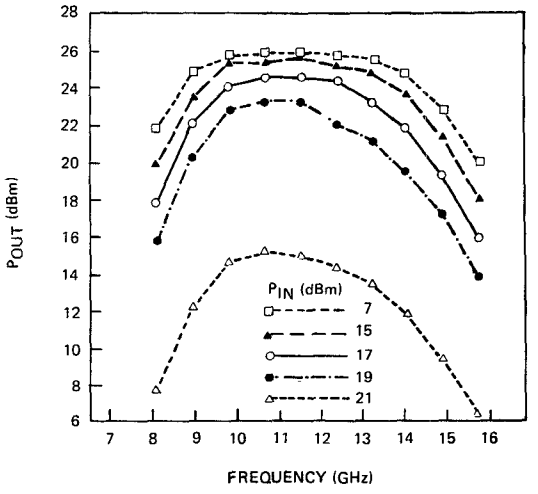


Fig. 17. Simulated P_{out} versus frequency curves of amplifier A at five different P_{in}.

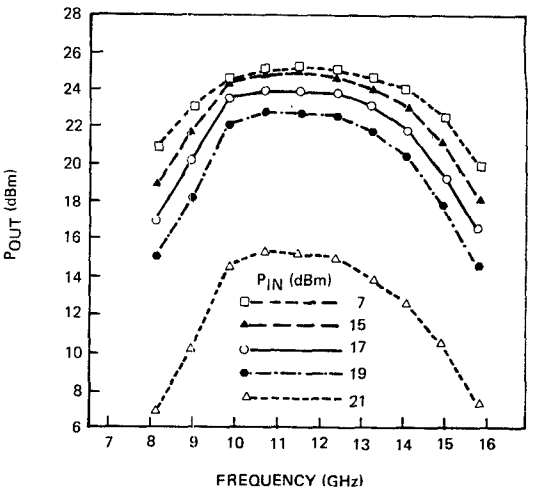


Fig. 18. Measured P_{out} frequency curves of amplifier A at five different P_{in}.

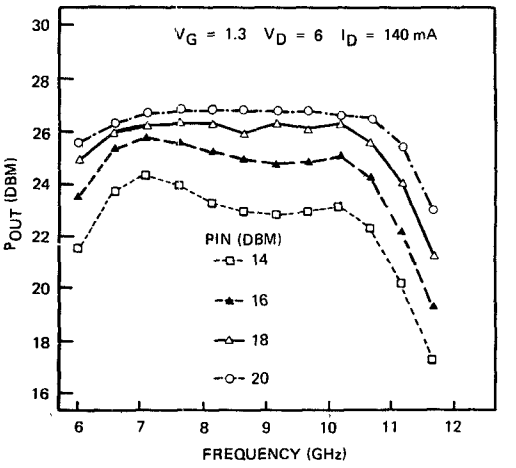


Fig. 19. Simulated P_{out} versus frequency curves of amplifier B at four different P_{in}.

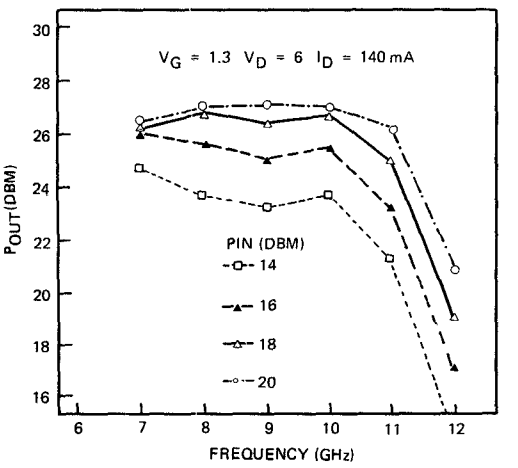


Fig. 20. Measured P_{out} versus frequency curves of amplifier B at four different P_{in}.

V. Results

Figs. 15 and 16 show the simulated and measured P_{out} versus P_{in} curves of amplifier A at 10.65 GHz for three different bias voltages. As shown, the model accurately predicts the saturation charateristics for different bias voltages. On the average, it takes four iterations to calculate each of these data points, and each iteration takes about 0.25 s of CPU time of a VAX-11/780 computer. Figs. 17 and 18 show the simulated and measured curves of P_{out} versus frequency of amlifier A at different input power levels. As shown, the difference between the simulation and measured data is within 1 dB across the frequency band for different input power levels. Figs. 19 and 20 are the simulated and measured P_{out} versus P_{in} curves of amplifier B. The difference between these two curves is within 0.5 dB. In Fig. 20, data below 7 GHz are not measured due to the limitation of the measurement setup.

VI. Conclusion

An accurate nonlinear MESFET model, an efficient large-signal analysis algorithm, and a reliable verification scheme are presented. The MESFET model is derived from RF measured data and is shown to be accurate at various bias voltages, frequencies, and input power levels. The waveform-balance method is used for nonlinear simulation. In this method, the closed-form Jacobian matrix is calculated in the time domain. The method is shown to have good convergence speed. To verify the model, two MMIC power amplifiers which use different MESFET devices are designed for use as test vehicles. In the verification scheme, the S parameters of the amplifiers' matching circuits are accurately measured using on-wafer probes. These S parameters are then directly used in the amplifier simulation. The agreement between measured and simulated data is excellent for both amplifiers.

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